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Paula Faulk Hurley
Paula Faulk Hurley

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Inventor:
Craig E. Hampel et al.

Application No. **10/766,761**

Filed: **28 January 2004**

Title: **Periodic Calibration for
Communication Channels by Drift
Tracking**

Group Art Unit: **2637**
Examiner: **Jayanti K. Patel**

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INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.56

Sir:

It is requested that the information identified in this statement be considered by the Examiner and made of record in the above-identified application. This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56.

Enclosed with this statement is Form PTO-SB/08. The Examiner is requested to initial the forms and return them to the undersigned in accordance with M.P.E.P. 609.

Also enclosed with this statement is a copy of each cited document as required by 37 C.F.R. 1.98. The exception to this, in accordance with the 05 August 2003 Official Gazette Notice in which the USPTO waives the requirement for submitting copies of U.S. Patent and Publications for cases filed after 30 June 2003, is that copies of U.S. Patent documents and copies of U.S. Patent publications are not being submitted.

This statement should be considered under 37 C.F.R. 1.97(b) because it is being filed before the mailing date of the first Office Action on the merits.

Fee Authorization. The Commissioner is hereby authorized to charge underpayment of any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0869 (RBUS 1309-1). A copy of this authorization is enclosed.

Respectfully submitted,

Date: 23 Jan 06

By: Mark A. Haynes

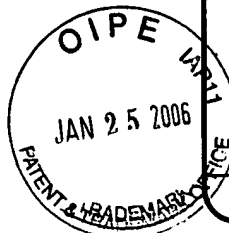
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	10/766,761
				Filing Date	28 January 2004
				First Named Inventor	Craig E. Hampel
				Group Art Unit	2637
				Examiner Name	Jayanti K. Patel
Sheet	1	of	2	Attorney Docket Number	RBUS 1309-1

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	A1	5,111,208		Lopez	05-05-1992	
	A2	6,163,570		Olafsson	12-19-2000	
	A3	6,173,345		Stevens	01-09-2001	
	A4	6,434,081		Johnson et al.	08-13-2002	
	A5	6,484,232		Olarig et al.	11-19-2002	
	A6	6,560,716		Gasparik et al.	05-06-2003	
	A7	6,606,576		Sessions	08-12-2003	
	A8	6,662,305		Salmon et al.	12-09-2003	
	A9	6,889,357		Keeth et al.	05-03-2005	
	A10	2003/0149991		Reidhead et al.	08-07-2003	
	A11	2004/0217881		Carlson	02-06-2003	
	A12	2005/0163202		Hampel et al.	07-28-2005	
	A13					
	A14					
	A15					
	A16					
	A17					
	A18					
	A19					
	A20					

FOREIGN PATENT DOCUMENTS								
Examiner Initials ¹	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	To
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
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	B9							
	B10							

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			Application Number	10/766,761	
			Filing Date	28 January 2004	
			First Named Inventor	Craig E. Hampel	
			Group Art Unit	2637	
			Examiner Name	Jayanti K. Patel	
Sheet	2	of	2	Attorney Docket Number	RBUS 1309-1

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
	C1	EIA/JEDEC Standard No. 8-B (JESD8-B) "Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits," (Sept. 1999) 12 pages.	
	C2	EIA/JEDEC Standard No. 8-6 (EIA/JESD8-6) "High Speed Transceiver Logic (HSTL) A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits," (Aug. 1995) 16 pages.	
	C3	JEDEC Standard - JESD8-16 "Bus Interconnect Logic (BIC) for 1.2 Volts," (Apr. 2004) 16 pages.	
	C4	LEE, Ming-Ju Edward et al., "TP 15.3: A 90mW 4Gb/s Equalized I/O Circuit with Input Offset Cancellation" IEEE International Solid-State Circuits Conference, pages 252-253.	

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